WHAT IS CLAIMED IS:

1. A method for verifying frequency of a clock signal, said clock signal having a first period T1, said method comprises steps of:

frequency-dividing said clock signal into a bi-level divided clock signal with a second period T2 in response to a reset signal, where T2/n = T1 and n is greater than unity;

detecting a level of said bi-level divided clock signal per predetermined period Ts in response to said reset signal;

calculating a period deviation range Te of said clock signal when said bi-level divided clock signal is detected to be a first level from the first to the (p-q)th detected points but a second level at the (p+1)th detected point; and

verifying frequency of said clock signal according to said period deviation range Te of said clock signal.

2. The method according to claim 1 wherein p = T2/(2*Ts), q = T1/Ts, and Te = (q+(1/2))*Ts/(n/2).

3. The method according to claim 1 wherein said period deviation range Te of said clock signal is calculated when said bi-level divided clock signal is detected to be said first level from the first to the (p-q)th detected points, to be said second level from the (p+1)th to the (2p-q) detected points, and to be said first level at the (2p+1) detected point.

4. The method according to claim 3 wherein p = T2/(2*Ts), q = T1/Ts, and Te = (q+(1/2))*Ts/n.

5. The method according to claim 3 wherein said period deviation range Te of said clock signal is calculated when said bi-level divided clock signal from the first to the (mp+1)th detected points are detected to be at predetermined levels, and said period deviation range Te is defined by a formula Te =

(q+(1/2))*Ts/(m*n/2), where m is a positive integer.

6. The method according to claim 1 wherein said predetermined period Ts is a time period between two adjacent rising edges of a reference clock signal, and a level change of said reset signal occurs at a falling edge of said reference clock signal.

7. The method according to claim 1 wherein Ts is no greater than T1.

8. A method for verifying frequency of a clock signal generated from a clock signal generator, said clock signal having a first period T1, said method comprising steps of:

frequency-dividing said clock signal into a bi-level divided clock signal with a second period T2 in response to a reset signal, wherein T2/n = T1, and n is a frequency-dividing parameter;

detecting said bi-level divided clock signal in response to said reset signal and a reference clock signal having a third period Ts; and

determining said clock signal generator to be in a normal operating state when a predetermined number m of continuous level changes of said bi-level divided clock signal all occur at specified ranges; and

calculating a period deviation range Te of said clock signal according to a parameter q for defining said specified ranges, said third period Ts, said predetermined number m and said frequency-dividing parameter n when said clock signal generator is determined to be said normally operating state.

9. The method according to claim 8 wherein Te = (q+(1/2))*Ts/(m*n/2).

10. The method according to claim 8 wherein rising and falling edges of said reset signal are consistent with a falling edge of said reference clock signal.

11. The method according to claim 8 wherein a first and a second level changes of said bi-level divided clock signal occurs at specified ranges are determined

when said bi-level divided clock signal is detected to be a first level from the first to the (p-q)th detected points, to be a second level from the (p+1)th to the (2p-q) detected points, and to be said first level at the (2p+1) detected point.

12. The method according to claim 11 wherein p = T2/(2*Ts) and q = T1/Ts.

13. A device for verifying frequency of a clock signal generated from a clock signal generator, comprising:

a reference signal generator for providing a reference clock signal and a reset signal;

a frequency divider in communication with said reference signal generator and said clock signal generator, receiving and frequency-dividing said clock signal into a bi-level divided clock signal in response to said reset signal; and

a comparative detector in communication with said frequency divider and said reference signal generator, detecting a level of said bi-level divided clock signal in response to said reset signal and said reference clock signal, and verifying frequency of said clock signal according to a period deviation range Te when said bi-level divided clock signal is detected to be a first level from the first to the (p-q)th detected points but a second level at the (p+1)th detected point.

14. The device according to claim 13 wherein Te = (q+(1/2))*Ts/(n/2).

15. The device according to claim 13 wherein said comparative detector verifies frequency of said clock signal according to said period deviation range Te when said bi-level divided clock signal is detected to be said first level from the first to the (p-q)th detected points, to be said second level from the (p+1)th to the (2p-q) detected points, and to be said first level at the (2p+1) detected point, and said period deviation range Te is defined by a formula Te = (q+(1/2))*Ts/n.

16. The device according to claim 13 wherein said comparative detector verifies frequency of said clock signal according to said period deviation range

Te when said bi-level divided clock signal from the first to the (mp+1)th detected points are detected to be at predetermined levels, and said period deviation range Te is defined by a formula Te = (q+(1/2))*Ts/(m*n/2), where m is a positive integer.

17. The device according to claim 13 wherein said level of said bi-level divided clock signal is detected in response to said reset signal and a rising edge of said reference clock signal, and a level change of said reset signal occurs at a falling edge of said reference clock signal.